I Semester [VLSI Design & Embedded Systems]

USN | | | | | | | | | | |

12EC130

M.Tech. Degree Examination, Dec.2013/Jan.2014

VLSI Design Verification

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Discuss the importance of verification in VLSI design. Why formal methods are a preferred way of verification? **(10 Marks)**

b. How verification time may be reduced? **(05 Marks)**

c. What is reconvergent model of verification? Give some examples. **(05 Marks)**

2 a. Describe linting process with help of following code:

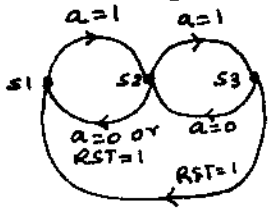
```
module abc (a, b, c);
   input a, b;
   output c;
   reg c;
   if (a = = 2'b01)
      c < = T'b1;
   if (b = T'b0)
      c = T'b0;
end module
```

(10 Marks)

b. Compare testing and verification. **(05 Marks)**

c. Briefly explain the model checking process. **(05 Marks)**

3 a. Explain the terms:
i) FSM coverage,
ii) Statement coverage and
iii) Transition coverage.
Write a test for the following FSM. State any assumptions made.



FSM for Q3(a) **(10 Marks)**

b. What are code metrics? Give some examples. **(05 Marks)**

c. Discuss how ASIC verification is performed. **(05 Marks)**

4 a. For the following code, write verification code. Highlight its statement coverage.

```
module HA (a, b, c, s)
   input a, b;
   output c, s;
   reg c, s;
   xor (s, a, b);
   and (c, a, b);
end module
```

(10 Marks)

b. Give schematic of a typical RC timing model of a CMOS gate. **(05 Marks)**

c. What is unateness of a signal? Explain with suitable waveforms. **(05 Marks)**

5 a. Justify the need for a verification specification document. Describe its functionality and usage. **(10 Marks)**

b. Give an example of timing description of an output pin in NDLM format. **(05 Marks)**

c. What is the need for parasitic extraction and how it is used in back annotation? **(05 Marks)**

6 a. Discuss the effect of IR drop in signal integrity. **(05 Marks)**

b. Give an overview of design sign off process. **(05 Marks)**

c. Discuss various timing parameters used in a static timing analysis. **(05 Marks)**

d. Describe setup and hold times. **(05 Marks)**

7 a. Why ordering of variables is critical for drawing a ROBDD? **(05 Marks)**

b. Draw ROBDD for the function $f = abc + a'bc' + a'b'c + a'b'c'$. **(10 Marks)**

c. What are SAT solvers? **(05 Marks)**

8 Write short notes on any FOUR:

a. Equivalence checking

b. Signal integrity

c. Event based simulators

d. Design rules for digital VLSI

e. Waveform skew measurements

f. Antenna effects during plasma etch. **(20 Marks)**

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